REMARKS

Claims 1-19 of the subject application are currently pending, and have been rejected by the Examiner. In the accompanying amendment, claims 1, 5, 6, 8, 9, 12, 13, 15, 18, and 19 have been amended. The amendments to the claims are supported by the written description, claims, and drawings as originally filed, and therefore do not add new matter.

Drawings

The Examiner has objected to Figures 1, 2, and 5. In particular, the Examiner has stated that "the drawings are objected to because Figures 1, 2, and 5 should be designated by a legend such as – prior art – because only that which is old is illustrated". Applicant, respectfully disagrees with the Examiner because Figures 1, 2, and 8 do not illustrate only that which is old. As described in paragraph 14 of the subject application, Figure 1 shows a system 10 which includes system hardware 12 described with reference to Figure 5 of the drawings. As will be seen from paragraph 27 of the subject application, the system hardware 12 includes a memory 502 which includes instructions 504 which when executed by a processor 500 cause the processor to perform the methodology of the invention. Thus, to the extent that the systems of Figures 1, and 5 include instructions to perform the methodology of the invention, it is respectfully submitted that the systems of Figures 1, and 5 are not prior art. Further, the flowchart of operations shown in Figure 2 of the drawings includes operations that are not part of the prior art. For example, the operation 104 to generate compensation code is not part of the prior art, hence the flowchart of Figure 2 is not prior art. Based on the foregoing, the Examiner is respectfully requested to withdraw his objection to Figures 1, 2, and 5.

Claim Objections

The Examiner objected to claims 1, 8, and 15 because of minor informalities. With regard to claim 1, the Examiner required an insertion of a colon after the word

"comprising". In response, the Applicant has amended claim 1 to include a colon after the word "comprising". With regard to claims 1, 8, and 15, the Examiner has indicated that the term "and to" should be added between "the source code block" and "access to the updated memory locations" in order to clarify the meaning of the limitation. Applicant respectfully points out to the Examiner that if claims 1, 8, and 15 were to be amended as suggested by the Examiner, then the limitation would read "the source code block and to access to the updated memory locations", which would not make any sense. In this regard, the Applicant believes that the Examiner perhaps has misread the limitations of claim 1, 8, and 15 and points out to the Examiner that access to the updated memory locations is provided to the native code. Consequently, the Applicant has amended claims 1, 8, and 15 to insert a "," after "native code", and before "corresponding" to clearly indicate that access to the updated memory locations is provided to the native code. On account of the foregoing, the Examiner is respectfully requested to withdraw his objection to claims 1, 8, and 15.

Claim Rejections Under 35 U.S.C. § 112

The Examiner has objected to claims 5, 9, and 18 under 35 U.S.C. § 112. In response, the Applicant has amended these claims and respectfully submits, that by virtue of the amendments to the claims, the claims are now not objectionable under 35 U.S.C. § 112.

Regarding claims 6, and 13, the Examiner objected to the use of the trademark "Java" in these claims. In response, the Applicant has amended these claims to remove the term "Java". With regard to claims 7, and 14, the Examiner objected to the use of the term "Just-In-Time" on the ground that the term is a trademark. At the time of preparing the patent application, the Applicant believed that the term "Just-In-Time" was a trademark of Sun Microsystems Inc. of Palo Alto, California. However, upon subsequent enquiry, the term "Just-In-Time" is not a trademark and accordingly it is believed that the use of the term in the claims is proper.

Based on the foregoing, the Examiner is respectfully requested to withdraw his rejection of claims 6, 7, 13, and 14.

Claim Rejections Under 35 U.S.C. § 101

The Examiner has rejected claims 15-19 under 35 U.S.C. § 101 as being directed to non statutory subject matter. In this regard, the Examiner has stated that claim 15 "while reciting an apparatus comprising a processor, a memory coupled thereto (i.e. hardware components), and identifier, transformer and a compensator (i.e. software components) fails to indicate that the software components are stored on the memory and executed by the processor. As recited, claim 15 fails to indicate that the software components are tangibly embodied and executed by a piece of hardware and that their functions have practical applications which produce useful, concrete, and tangible results under the State Street formulation".

In response, the Applicant has amended claim 15 to clearly indicate that the identifier, transformer, and compensator are eligibly embodied and executed by a piece of hardware. Accordingly, the Examiner is respectfully requested to withdraw his rejection of claim 15 under 35 U.S.C. § 101. Given that claims 16-19 depend on claim 15, it is respectfully submitted that these claims also comply with 35 U.S.C. § 101.

Claim Rejections Under 35 U.S.C. § 102

The Examiner has rejected claims 1-3, 6-7, 8-10, 13-14, and 15-17 under 35 U.S.C. § 102(b). In particular, the Examiner argues that the limitation of claim 1 comprising:

> "generating compensation native code to update each memory location with a value from an associated register to provide native code, corresponding to a source code exception handler associated with the source code block accessed to the updated memory locations".

Forms part of the admitted prior art by virtue of paragraphs 003-007 of the subject application. Applicant, however, respectfully disagrees with the Examiner in this regard. Applicant argues that paragraphs 003-007 describe how register promotion is

performed in the prior art but does not admit that the step of "generating compensation native code to update each memory location with a value from an associated register to provide native code, corresponding to a source code exception handler associated with the source code block, accessed to the updated memory locations" is part of the prior art. Thus, the Examiner is incorrect in arguing that the step of generating compensation code, as recited in claim 1 is part of prior art.

Based on the foregoing, the Examiner is respectfully requested to withdraw his rejection of claim 1, and its dependent claims 2-19.

It is respectfully submitted that in view of the amendments and remarks set forth herein, all rejections have been overcome. All pending claims are now in condition for allowance, which is earnestly solicited.

Authorization is hereby given to charge our Deposit Account 02-2666 for any charges that may be due. Furthermore, if an extension is required, then Applicant hereby requests such an extension.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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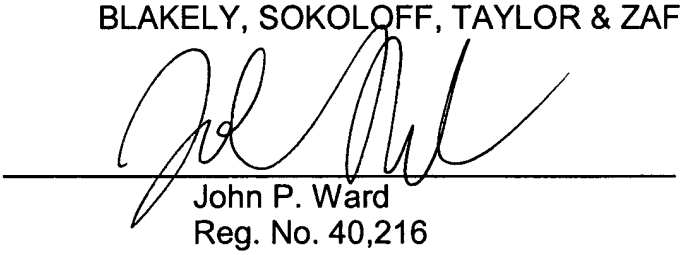

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